UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/334,646	06/17/1999	SHUNPEI YAMAZAKI	0756-1984	5565

31780 7590 05/25/2005

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

5/21

Office Action Summary	Application No.	Applicant(s)	
	09/334,646	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,11-14,16,38-41,58,59,71,72,78,79,100,101 and 122-145* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,11-14,16,38-41,58,59,71,72,78,79,100,101 and 122-145* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20030618*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-2, 11-14, 16, 38-41, 58-59, 71-72, 78-79, 100-101 and 122-145 are objected to because of the following informalities and/or defects:

Claims 1-2, 122, 128, 134 and 140 each recite or implicate the subject matters that the channel-forming regions of the recited two transistors are in two separated semiconductor layers. However, among various possible interpretations, such limitations may be interpreted as meaning: the two transistor for formed of two different semiconductor layers (on different levels), even though they may both be formed in contact with a same insulating surface. For example, two separated film layers may be displaced on two different levels but can still be in contact with a same insulation layer that has an uneven or tilt surface. It would then be unreadable on the specification and the drawings (see Fig. 3) of the instant disclosure, since the channel regions of the two transistors therein are formed of two separated regions of a same semiconductor layer.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 11-14, 16, 71-72, 78-79, 122-125, 127-131, 133-137, 139-143 and 145, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over by Kato (US 5,589,406; of record) in view of EP'749 (Yamazaki et al., EP 0 502 749 B1; of record) and/or Matsueda (US 5,173,792; of record).

Kato discloses an active matrix type LC display device having a buffer circuit in the drive circuit (Figs. 1-13, esp. Figs. 7 and 12; also see col. 13, lines 5-50), comprising: a first TFT (the middle one of 10D1(i)) and second TFT (the lower one of 10D1(i)), wherein the two TFTs share a common gate electrode, a common source electrode and a common drain electrode, and the two channel forming regions of the two TFTs are formed in separated regions of a Si layer that is naturally on a same insulating surface.

In addition, it is noted that an active matrix type LC device such as the one of Kato naturally further comprises a memory and a decode. And the channel-forming regions in the thin Si film therein naturally have point defects.

Kato does not expressly disclose that the two parallel-connected TFTs can be arranged in the channel width direction. However, as evidenced in EP'749 (Figs. 13 and 14) and/or Matsueda (Figs. 2-4, 7, 9 and 11), one of ordinary skill in the art would readily recognize that such arrangement is also a common one for forming a parallel connection of two TFTs, and/or that the resulting layout of such arrangement is tighter, simpler, and/or more straight forward, compared with the parallel-connected TFTs arranged along the channel length direction.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the TFT device of Kato with the parallel-connected TFTs being arranged in the channel width direction, per the teachings of EP'749 and/or Matsueda, so that a TFT device with another common parallel connection layout for the parallel-connected TFTs and/or with a TFT parallel connection layout that is tighter, simpler, and/or more straight forward, would be obtained.

Regarding claims 124, 130, 136 and 142, the common gate, source and drain electrodes for the two TFTs in Kato are all extended in parallel with each other along the vertical direction (see Fig. 12).

4. Claims 38-41, 58-59, 100-101, 126, 132, 138 and 144, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kato in view of EP'749 and/or Matsueda, and further in view of Zhang (US 5,403,772; of record).

The disclosures of Kato, EP'749 and Matsueda are discussed as applied to claims 1-2, 11-14, 16, 71-72, 78-79, 122-125, 127-131, 133-137, 139-143 and 145 above.

Although Kato in view of EP'749 and/or Matsueda does not expressly disclose that the silicon semiconductor layer can be monocrystalline, one of ordinary skill in the art would readily recognize that monocrystalline silicon can be desirably formed for improving the performance of the TFTs, as evidenced in Zhang as explained below.

Zhang teaches to form an active matrix type LC display device (Figs. 1-8A, particularly, Fig. 8A), comprising: a pixel matrix portion (104) having a plurality of pixels

on an insulating substrate (107); and a peripheral driver circuit portion (101 and 102) on the same insulation substrate, thin film transistors (TFTs) in the driver circuit portion each having a channel forming region in one of the separate semiconductor layers (11a and 11b) provided on an insulating surface, wherein the channel forming region is provided in a region which can be regarded as effectively monocrystalline silicon (see col. 6, lines 13-15); and, the channel forming region contains impurities (a type of point defects) of carbon, nitrogen and oxygen at a concentration less than 10^{18} cm^{-3}, which meets the limitation of each channel forming region "containing carbon and nitrogen at a concentration of $5x10^{18}$ cm^{-3} or less, respectively, and containing oxygen at a concentration of $5x10^{19}$ cm^{-3} or less" recited in the claimed invention. It is noted that, since the channel forming region in Zhang is formed with a method which is substantially the same as the one used in the claimed invention, the method used in Zhang is regarded as being inherently capable of forming the channel forming region having no linear defects or surface defects. In addition, one of ordinary skill in the art would readily recognize that it is always desirable to form the channel forming region having no linear defects or surface defects for achieving good channel performance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporated the monocrystalline silicon layer of Zhang into the TFT device of Kato in view of EP'749 and/or Matsueda, so that an active matrix type LC display with better TFT performance therein would be obtained.

Response to Arguments

5. Applicant's arguments with respect to the rejected claims above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
May 23, 2005

SHOUXIANG HU
PRIMARY EXAMINER